

METHOD FOR FORMING SEMICONDUCTOR DEVICE HAVING TRANSISTOR OF GATE ALL AROUND STRUCTURE

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Inventor(s): SONG SEUNG-HEON +

Applicant(s): SAMSUNG ELECTRONICS CO LTD +

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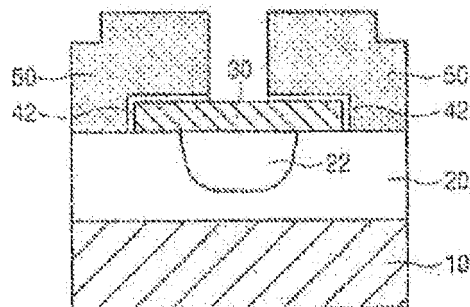
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Abstract of JP 2003037272 (A)

PROBLEM TO BE SOLVED: To provide a method for forming a semiconductor device having a GAA structure. **SOLUTION:** There are provided a stage, in which an SOI substrate composed of an SOI layer, an embedded oxide layer, and a lower-part substrate layer is prepared, a stage in which the SOI layer is patterned to form an active layer pattern, a stage in which an etching preventing film is laminated with a material having etching selective ratio relative to the embedded oxide layer and active layer pattern, on the active layer pattern, a stage in which the etching preventing film in a gate region, which crosses the active layer pattern at a channel region, is removed through patterning to form an etching preventing film pattern, so that the embedded oxide layer is exposed, a step in which the embedded oxide layer is etched isotropically with the etching preventing film pattern as etching mask, to form a cavity under the channel region of the active layer pattern, and a stage in which the cavity and the space between the etching preventing film patterns are filled with a conductive material.



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